SC4508A
Buck or Buck-Boost (Inverting) Current Mode Controller

Description

The SC4508A is a low voltage current mode switching regulator controller that drives a P-channel power MOSFET with programmable switching frequency. It can be configured in either buck or buck boost (inverting) converters. The converters can be operated from 2.7V to 15V input voltage range. The typical operating supply current is 3mA and a shutdown pin allows the user to turn the controller off reducing it to less than 200µA. The output voltage can adjusted by external resistor divider. The switching frequency is programmable up to 1.5MHz, allowing small inductor and capacitor values to minimize PCB space. The operating current level is programmable via an external sense resistor. Accessible reference voltage allows users to make output voltage as low as they want.

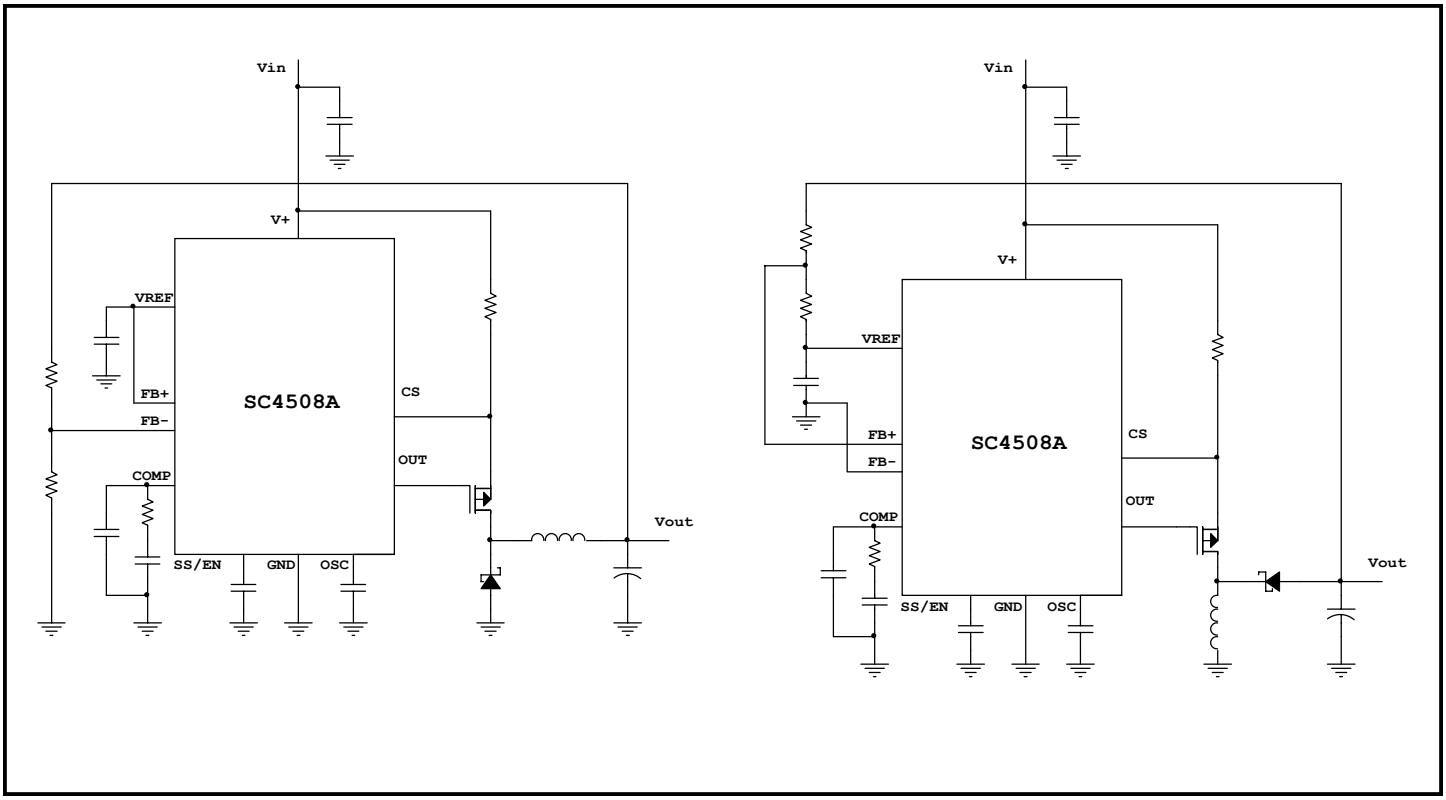
Features

- Wide input voltage range 2.7V to 15V
- Programmable output voltage
- Programmable switching frequency up to 1.5MHz
- Buck or buck boost (inverting) configuration
- Current mode control with slope compensation
- Very low quiescent current in shutdown mode
- Accessible reference voltage
- Hiccup mode after 32 cycle-by-cycle OCP
- 4mm x 4mm MLPQ-12 lead free package. This product is fully WEEE and RoHS compliant

Applications

- Low power point of use converters
- Single or multiple output low power converters
- Positive and/or negative output voltage
- DSL cards
- Graphic cards
- I/O cards
- Negative bias supplies

Typical Application Circuits



Absolute Maximum Rating

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
VDD to GND		-0.3 to 16	V
SS/EN to GND(1)		3.2	V
FB+, FB-, COMP, OSC to GND		5	V
VREF Current		1	mA
Thermal Resistance, Junction to Ambient	θ_{JA}	48	°C/W
Thermal Resistance, Junction to Case	θ_{JC}	3	°C/W
Storage Temperature Range	T_{STG}	-60 to +150	°C
Junction Temperature Range	T_J	-40 to +150	°C
Peak IR Reflow Temperature 10 - 40s	T_{PKG}	260	°C

Note: (1) Voltage from internal circuitry could be higher than 3.2V. See Application Information, Soft-Start section.

Electrical Characteristics

Unless specified: V_{DD} = 12V, V_{FB+} = V_{REF}, V_{FB-} = 0, OUT = open, C_{VDD} = 1uF, $C_{SS/EN}$ = 0.1uF, C_{OSC} = 330pF. T_A = T_J = -40°C to 125°C

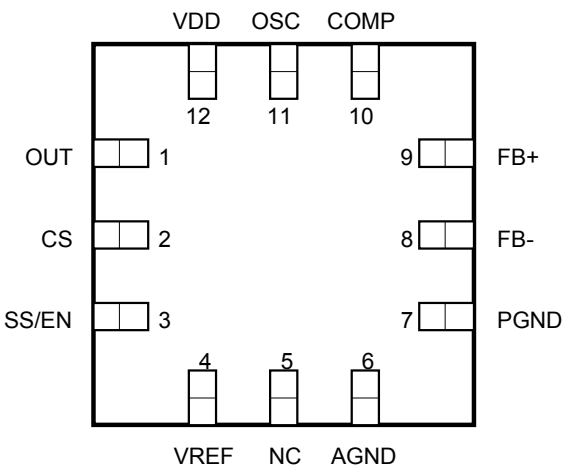
Parameter	Test Conditions	Min	Typ	Max	Unit
Power Supply					
Input Voltage Range		2.7		15	V
Quiescent Current	SS/EN = low		200	500	µA
Operating Current	SS/EN = high, No load		3		mA
Undervoltage Lockout					
Start Threshold	V_{DD} rising	2.35	2.5	2.55	V
UVLO Hysteresis			100		mV
Oscillator					
Frequency Range		100		1500	KHz
Frequency		450	500	550	KHz
Charge Current			100		µA
Error Amplifier					
Feedback Input Voltage		-0.2		0.7	V
Offset Voltage			2		mV
Input Bias Current			100	300	nA
Transconductance			5		mS
Output Source or Sink Current		50	100		µA

Electrical Characteristics (Cont.)

Unless specified: V_{DD} = 12V, V_{FB+} = V_{REF}, V_{FB-} = 0, OUT = open, C_{VDD} = 1uF, $C_{SS/EN}$ = 0.1uF, C_{OSC} = 330pF. T_A = T_J = -40°C to 125°C

Parameter	Test Conditions	Min	Typ	Max	Unit
PWM Comparator					
Maximum Duty Cycle	C = 1.5nF, 100kHz		97		%
	C = 100pF, 1.5MHz		95		%
Minimum On Time			200		nS
Slope Compensation			63		mV/Ts
Delay to Output			50		ns
VREF Reference					
Output Voltage		0.4925	0.5	0.5075	V
Output Voltage	T_A = 25°C, V_{DD} = 5V	0.496	0.5	0.504	V
Output Current				1	mA
Line Regulation	V_{DD} = 2.7 to 15V, I_{VREF} = 1mA		5	10	mV
Load Regulation	V_{DD} = 5V, I_{VREF} = 0 to 1mA		2	4	mV
Soft Start/Enable/Shutdown					
Charge Current	$V_{SS/EN}$ > 0.9V		20		µA
	$V_{SS/EN}$ < 0.9V		10		
Discharge Current			12		mA
Enable Logic Voltage		2			V
SHDN Logic Voltage				0.35	V
Current Limit					
Cycle by Cycle Threshold	V_{DD} = 5V	90	110	130	mV
Consecutive Overcurrent Clock Cycles before Auto Restart Shutdown			32		
Delay to Output			50		nS
Output					
Gate Drive On-Resistance(H)			8		Ohm
Gate Drive On-Resistance(L)			8		Ohm
Gate Drive On-Resistance(H)	V_{DD} = 5V		15		Ohm
Gate Drive On-Resistance(L)	V_{DD} = 5V		15		Ohm
Rise Time	C_{OUT} = 1000pF		20		nS
Fall Time	C_{OUT} = 1000pF		20		nS

Pin Configuration



(MLPQ - 12, 4mm x 4mm)

Ordering Information

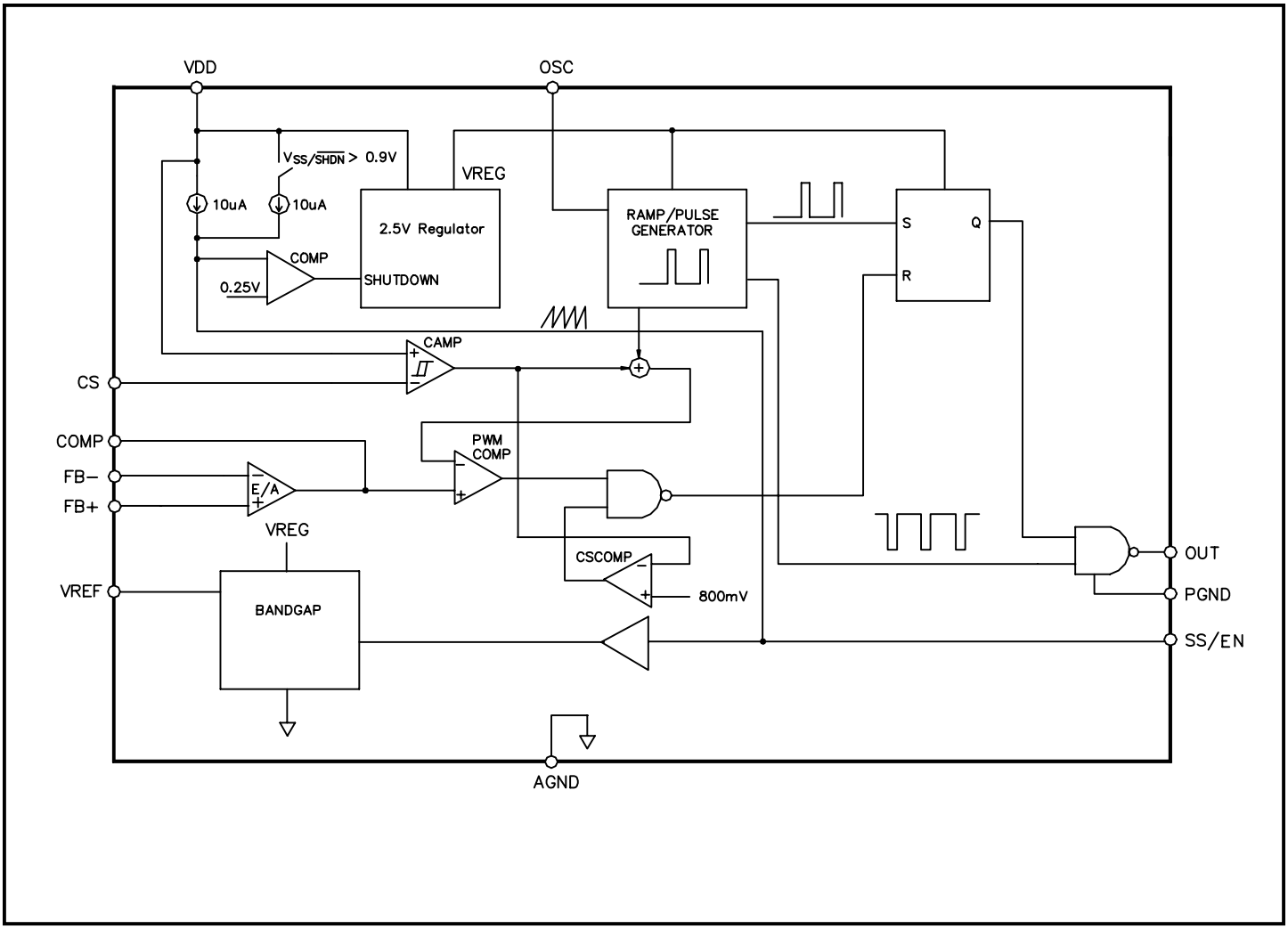
Part Number	Package (1)
SC4508AMLTRT(2)	MLPQ -12
SC4508ABUCKEVB	Evaluation Board
SC4508ABUCK-BOOSTEVB	Evaluation Board

Notes:
(1) Only available in tape and reel packaging. A reel contains 3000 devices.
(2) Lead free product. This product is fully WEEE and RoHS compliant.

Pin Descriptions

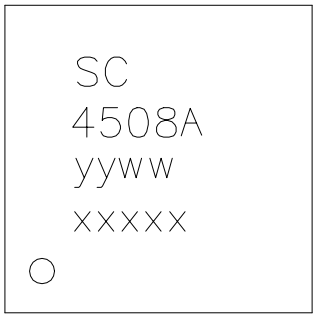
Pin #	Pin Name	Pin Function
1	OUT	Gate driver output for external P-MOSFET. OUT swings from VDD to PGND.
2	CS	Current sense input pin. Connect a current sense resistor between VDD and CS.
3	SS/EN	Soft start pin. Connects an external capacitor between this pin and AGND. The ramp up time is defined by the capacitor. The device goes into shutdown when VSS/EN is pulled below 0.25V.
4	VREF	0.5V reference output. VREF can source up to 1mA. Bypass with a 0.1uF ceramic capacitor from VREF to AGND.
5	NC	No connection.
6	AGND	Analog ground.
7	PGND	Power ground.
8	FB-	Error amplifier inverting input.
9	FB+	Error amplifier non-inverting input.
10	COMP	Compensation pin for internal transconductance error amplifier. Connect loop compensation network from COMP to AGND.
11	OSC	Oscillator frequency set input. Connect a ceramic capacitor from OSC to AGND to set the internal oscillator frequency from 100KHz to 1.5MHz. Use equation $f = \frac{100\mu A}{C \bullet 0.65}$ to set the oscillator frequency. C is the capacitor from OSC to AGND.
12	VDD	Supply voltage. Bypass a 1uF ceramic capacitor from VDD to PGND.
	THERMAL PAD	Pad for heatsinking purposes. Connect to ground plane using multiple vias. Not connected internally.

Block Diagram



Marking Information

Top View



yyww = Date Code (Example: 0012)

Application Information

The SC4508A is designed to control buck (step down) or buck-boost (inverting) converter with P-channel MOSFET as a switch using current mode, programmable switching frequency architecture. During steady state operation, the switch is turned on each cycle and turned off when the voltage across current sense resistor exceeds the voltage level at COMP pin set by voltage loop error amplifier. A fixed 0.5V artificial ramp is added internally to the amplified current signal for operations when duty-cycle is larger than 50%. In over load or output shortage condition, if the sensed current signal reaches typical 100mV, the switch is turned off immediately in the same cycle. If the sensed current signal continues up to 32 cycles, not only the switch is turned off but also the soft start capacitor is discharged by a internal MOSFET to ground then charging back to threshold 1.4V during which the switch is held off. With the "hiccup" mode over current protection, the thermal stress is reduced in the faulty conditions.

Frequency Setting

The switching frequency in the SC4508A is user-programmable. The advantages of using constant frequency operation are simple passive component selection and ease of feedback compensation. Before setting the operating frequency, the following trade-offs should be considered.

1) Passive component size
2) Circuitry efficiency
3) EMI condition
4) Minimum switch on time and
5) Maximum duty ratio

For a given output power, the sizes of the passive components are inversely proportional to the switching frequency, whereas MOSFET's/Diodes switching losses are proportional to the operating frequency. Other issues such as heat dissipation, packaging and the cost issues are also to be considered. The frequency bands for signal transmission should be avoided because of EM interference.

The free-running frequency of the internal oscillator can be programmed with an external capacitor from the OSC pin to the ground. The SC4508A controller is capable of operating up to 1.5 MHz. It is necessary to consider the operating duty-ratio before deciding the switching frequency.

Minimum Switch On Time Consideration

In the SC4508A the falling edge of the clock turns on the MOSFET. The inductor current and the sensed voltage ramp up. After the sensed voltage crosses a threshold determined by the error amplifier output, the MOSFET is turned off. The propagation delay time from the turn-on of the controlling MOSFET to its turn-off is the minimum switch on time. The SC4508A has a minimum on time of about 180ns at room temperature. This is the shortest on interval of the controlling PFET. The controller either does not turn on the MOSFET at all or turns it on for at least 80ns.

For a buck converter, the operating duty cycle is V_O/V_{IN}. So the required on time for the MOSFET is $V_O/(V_{IN}fs)$. If the frequency is set such that the required pulse width is less than 180ns, then the converter will start skipping cycles. Due to minimum on time limitation, simultaneously operating at very high switching frequency and very short duty cycle is not practical. If the voltage conversion ratio V_O/V_{IN} and hence the required duty cycle is higher, the switching frequency can be increased to reduce the sizes of passive components.

There will not be enough modulation headroom if the on time is simply made equal to the minimum on time of the SC4508A. For ease of control, we recommend the required pulse width to be at least 1.5 times the minimum on time.

Current Sense and Current Limit

The SC4508A senses peak inductor current by a current sense resistor. The sensed voltage is referenced to VDD and the typical current limit threshold is 100mV. The current sense resistor can be calculated by the following equation assuming the current limit is 20% above peak incuctor current:

$$Rs = \frac{100mV}{120\% \bullet I_L(pk)}$$

$$I_L(pk) = I_O + \frac{1}{2}\frac{V_{IN} - V_O}{f_s \bullet L}\left(\frac{V_O + V_D}{V_{IN} + V_D}\right) \text{ for Buck}$$

Application Information (Cont.)

$$I_L(pk) = I_O \frac{V_{IN} + |V_O| + V_D}{V_{IN}} + \frac{1}{2} \frac{V_{IN}}{f_s \bullet L} \left(\frac{|V_O| + V_D}{V_{IN} + |V_O| + V_D} \right)$$

for Buck – Boost

I_O - full load current
V_O - output voltage
V_{IN} - input voltage
V_D - diode forward voltage drop
f_S - switching frequency
L - inductor

Error Amplifier

The error amplifier in the SC4508A is a transconductance error amplifier, which is easily configured as a type two compensator by connecting compensation network from the COMP pin to AGND. The output voltage of the error amplifier is compared to the sensed current signal (amplified by gain 8) plus internal 500mV ramp to generate duty cycle.

Both the non-inverting and the inverting inputs of the error amplifier are brought out as device pins so that a converter can be configured as either buck or buck-boost converter.

Soft-Start and Overload Protection

The undervoltage lockout circuit discharges the SS/EN capacitors. After V_{DD} rises above 2.5V, the SS/EN capacitors are slowly charged by internal 10uA current source. As the SS/EN capacitor continues to be charged, the VREF and the COMP voltage follows. The converter gradually delivers increasing power to the output. The inductor current follows the COMP voltage envelope until the output goes into regulation.

After the SS/EN capacitor is charged above 1.4V (high enough for the error amplifier to provide full load current), the overload detection circuit is activated. If the CS pin senses 32 consective switching cycles of over current, the SC4508A will shut down and hold off the MOSFET while discharging the soft-start capacitor. The SS/EN capacitor is discharged with an internal 12mA current sink. The overload latch is reset when the SS/EN capacitor is discharged below 0.5V. The SS/EN capacitor is then recharged with the 10µA current source and the converter undergoes soft-start. If overload persists, the SC4508A will undergo repetitive auto-shutdown-restart hiccup mode.

In normal operation, the VREF voltage follows the SS/EN voltage from 0 to 0.5V as the SS/EN voltage ramps up from 1.4V to 1.9V. After the SS/EN voltage rises above 1.9V, it settles at final value depending upon VDD. If VDD higher than 7V, it is clamped around 6.8V. In the worst case, the clamped voltage is about 10V. Therefore, the external soft-start capacitor should be rated at least 16V.

The SS/EN pin can also be used as the enable input. The MOSFET will be turned off if the SS/EN pin is pulled below 0.5V.

Converter Specifications

Buck or buck-boost converter design includes the following specifications:

Input voltage range: $V_{in} \in [V_{in,min}, V_{in,max}]$
Input voltage ripple (peak-to-peak): DV_{in}
Output voltage: V_o
Output voltage accuracy: e
Output voltage ripple (peak-to-peak): DV_o
Nominal output (load) current: I_o
Maximum output current limit: $I_{o,max}$
Output (load) current transient slew rate: dI_o (A/s)
Circuit efficiency: h

Selection criteria and design procedures for the following are described.
1) output inductor (L) type and value
2) output capacitor (C_o) type and value
3) input capacitor (C_{in}) type and value
4) power MOSFETs
5) current sensing and limiting circuit
6) voltage sensing circuit
7) loop compensation network

Inductor (L) and Ripple Current

The output inductor selection/design is based on the output DC and transient requirements. Both output current and voltage ripples are reduced with larger inductors but it takes longer to change the inductor current during load transients. Conversely smaller inductors results in lower DC copper losses but the AC

Application Information (Cont.)

core losses (flux swing) and the winding AC resistance losses are higher. A compromise is to choose the inductance such that peak-to-peak inductor ripple-current is 20% to 30% of the rated output load current or the inductor DC current. Assuming that the inductor current ripple (peak-to-peak) value is $\Delta I_L = \delta$ *Idc, the inductance value will then be:

$$L = \frac{V_{IN} - V_O}{f_s \bullet \Delta I_L}\left(\frac{V_O + V_D}{V_{IN} + V_D}\right) \text{ for Buck}$$

$$L = \frac{V_{IN}}{f_s \bullet \Delta I_L}\left(\frac{|V_O| + V_D}{V_{IN} + |V_O| + V_D}\right) \text{ for Buck-Boost}$$

The peak current in the inductor becomes (1+δ/2)*Idc and the RMS current is:

$$I_{L,rms} = I_{dc}\sqrt{1 + \frac{\delta^2}{12}}$$

The Idc is the inductor average or DC current.
The following are to be considered when choosing inductors:

a) Inductor core material: For high efficiency applications above 350KHz, ferrite, Kool-Mu and polypermalloy materials should be used. Low-cost powdered iron cores can be used for cost sensitive-applications below 350KHz but with attendant higher core losses.
b) Select inductance value: Sometimes the calculated inductance value is not available off-the-shelf. The designer can choose the adjacent (larger) standard inductance value. The inductance varies with temperature and DC current. It is a good engineering practice to re-evaluate the resultant current ripple at the rated DC output current.
c) Current rating: The saturation current of the inductor should be at least 1.5 times of the peak inductor current under all conditions.

Output Capacitor (C_o) and V_{out} Ripple

The output capacitor provides output current filtering in steady state and serves as a reservoir during load transient. The output capacitor can be modeled as an ideal capacitor in series with its parasitic ESR (R_{esr}) and ESL (L_{esl}) (Figure 1).

Figure 1. An equivalent circuit of C_o

If the current through the branch is $i_b(t)$, the voltage across the terminals will then be:

$$v_o(t) = V_o + \frac{1}{C_o}\int_0^t i_b(t)dt + L_{esl}\frac{di_b(t)}{dt} + R_{esr}i_b(t)$$

This basic equation illustrates the effect of ESR, ESL and C_o on the output voltage.

The first term is the DC voltage across C_o at time *t=0*. The second term is the voltage variation caused by the charge balance between the load and the converter output. The third term is voltage ripple due to ESL and the fourth term is the voltage ripple due to ESR. The total output voltage ripple is then a *vector* sum of the last three terms.

Since the inductor current is a triangular waveform in buck configuration with peak-to-peak value $\delta * I_o$, the ripple-voltage caused by inductor current ripples is:

$$\Delta v_C \approx \frac{\delta I_o}{8C_o f_s}$$

the ripple-voltage due to ESL is:

$$\Delta v_{ESL} = L_{esl} f_s \frac{\delta I_o}{D}$$

and the ESR ripple-voltage is:

$$\Delta v_{ESR} = R_{esr}\delta I_o$$

Aluminum capacitors (e.g. electrolytic, solid OS-CON, POSCAP, tantalum) have high capacitances and low ESL's. The ESR has the dominant effect on the output ripple voltage. It is therefore very important to minimize the ESR.

Application Information (Cont.)

When determining the ESR value, both the steady state ripple-voltage and the dynamic load transient need to be considered. To keep the steady state output ripple-voltage < ΔV_o, the ESR should satisfy:

$$R_{esr1} < \frac{\Delta V_o}{\delta I_o}$$

To limit the dynamic output voltage overshoot/ undershoot within α (say 3%) of the steady state output voltage) from no load to full load, the ESR value should satisfy:

$$R_{esr2} < \frac{\alpha V_o}{I_o}$$

Then, the required ESR value of the output capacitors should be:

$$R_{esr} = \min\{R_{esr1}, R_{esr2}\}$$

The voltage rating of aluminum capacitors should be at least 1.5V_o. The RMS current ripple rating should also be greater than:

$$\frac{\delta I_o}{2\sqrt{3}}$$

Usually it is necessary to have several capacitors of the same type in parallel to satisfy the ESR requirement. The voltage ripple cause by the capacitor charge/ discharge should be an order of magnitude smaller than the voltage ripple caused by the ESR. To guarantee this, the capacitance should satisfy:

$$C_o > \frac{10}{2\pi f_s R_{esr}}$$

Buck-boost converter has higher ripple current than buck in output. The RMS value is the most important factor to consider. It has to be less than the output capacitor ripple current rating.

The buck-boost output capacitor RMS current is:

$$I_{RMS\_CAP} \approx I_O \sqrt{\frac{V_O + V_d}{V_{IN}}}$$

$$\Delta v_{ESR} = R_{esr} \cdot I_d$$

where, V_d and I_d are rectifier forward voltage and current.

In many applications, several low ESR ceramic capacitors are added in parallel with the aluminum capacitors in order to further reduce ESR and improve high frequency decoupling. Because the values of capacitance and ESR are usually different in ceramic and aluminum capacitors, the following remarks are made to clarify some practical issues.

Remark 1: High frequency ceramic capacitors may not carry most of the ripple current. It also depends on the capacitor value. Only when the capacitor value is set properly, the effect of ceramic capacitor low ESR starts to be significant.

For example, if a 10µF, 4mΩ ceramic capacitor is connected in parallel with 2x1500µF, 90mΩ electrolytic capacitors, the ripple current in the ceramic capacitor is only about 42% of the current in the electrolytic capacitors at the ripple frequency. If a 100µF, 2mΩ ceramic capacitor is used, the ripple current in the ceramic capacitor will be about 4.2 times of that in the electrolytic capacitors. When two 100µF, 2mΩ ceramic capacitors are used, the current ratio increases to 8.3. In this case most of the ripple current flows in the ceramic decoupling capacitor. The ESR of the ceramic capacitors will then determine the output ripple-voltage.

Remark 2: The total equivalent capacitance of the filter bank is not simply the sum of all the paralleled capacitors. The total equivalent ESR is not simply the parallel combination of all the individual ESRs either. Instead they should be calculated using the following formulae.

$$C_{eq}(\omega) := \frac{(R_{1a}+R_{1b})^2\omega^2 C_{1a}{}^2 C_{1b}{}^2 + (C_{1a}+C_{1b})^2}{(R_{1a}{}^2 C_{1a} + R_{1b}{}^2 C_{1b})\omega^2 C_{1a} C_{1b} + (C_{1a}+C_{1b})}$$

$$R_{eq}(\omega) := \frac{R_{1a}R_{1b}(R_{1a}+R_{1b})\omega^2 C_{1a}{}^2 C_{1b}{}^2 + (R_{1b}C_{1b}{}^2 + R_{1a}C_{1a}{}^2)}{(R_{1a}+R_{1b})^2\omega^2 C_{1a}{}^2 C_{1b}{}^2 + (C_{1a}+C_{1b})^2}$$

where R_{1a} and C_{1a} are the ESR and capacitance of electrolytic capacitors, and R_{1b} and C_{1b} are the ESR and capacitance of the ceramic capacitors respectively. (Figure 2)

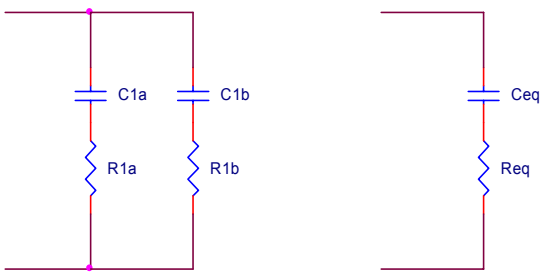


Figure 2. Equivalent RC branch.

Application Information (Cont.)

Req and Ceq are both functions of frequency. For rigorous design, the equivalent ESR should be evaluated at the ripple frequency for voltage ripple calculation when both ceramic and electrolytic capacitors are used. If $R_{1a} = R_{1b} = R_1$ and $C_{1a} = C_{1b} = C_1$, then R_{eq} and C_{eq} will be frequency-independent and

$$R_{eq} = 1/2\ R_1 \text{ and } C_{eq} = 2C_1$$

Input Capacitor (C_{in})

The input supply to the converter usually comes from a pre-regulator. Since the input supply is not ideal, input capacitors are needed to filter the current pulses at the switching frequency. A simple buck converter is shown in Figure 3.

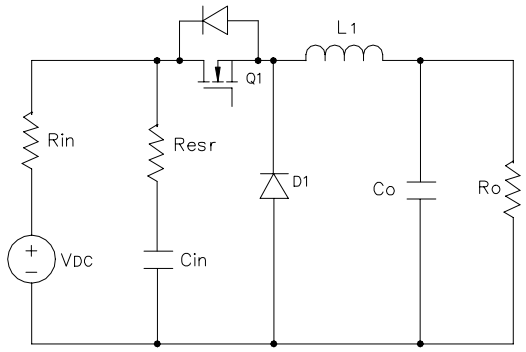


Figure 3. A simple model for the converter input

In Figure 3 the DC input voltage source has an internal impedance R_{in} and the input capacitor C_{in} has an ESR of R_{esr}. MOSFET and input capacitor current waveforms, ESR voltage ripple and input voltage ripple are shown in Figure 4.

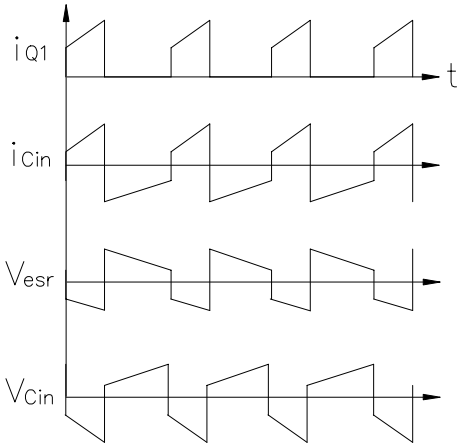


Figure 4. Typical waveforms at converter input.

It can be seen that the current in the input capacitor pulses with high di/dt. Capacitors with low ESL should be used. It is also important to place the input capacitor close to the MOSFETs on the PC board to reduce trace inductances around the pulse current loop.

The RMS value of the capacitor current is approximately

$$I_{Cin} = I_o\sqrt{D[(1+\frac{\delta^2}{12})(1-\frac{D}{\eta})^2 + \frac{D}{\eta^2}(1-D)]}$$

The power dissipated in the input capacitors is then:

$$P_{Cin} = I_{Cin}{}^2 R_{esr}$$

For reliable operation, the maximum power dissipation in the capacitors should not result in more than 10°C of temperature rise. Many manufacturers specify the maximum allowable ripple current (RMS) rating of the capacitor at a given ripple frequency and ambient temperature. The input capacitance should be high enough to handle the ripple current. For higher power applications, multiple capacitors are placed in parallel to increase the ripple current handling capability.

Sometimes meeting tight input voltage ripple specifications may require the use of larger input capacitance. At full load, the peak-to-peak input voltage ripple due to the ESR is:

$$\Delta v_{ESR} = R_{esr}(1+\frac{\delta}{2})I_{dc}$$

The peak-to-peak input voltage ripple due to the capacitor is:

$$\Delta v_C \approx \frac{DI_{dc}}{C_{in} f_s}$$

From these two expressions, C_{IN} can be found to meet the input voltage ripple specification.

Power MOSFETs Selection

Main considerations in selecting the MOSFETs are power dissipation, cost and packaging. Switching losses and conduction losses of the MOSFETs are directly related to the total gate charge (C_g) and channel on-resistance ($R_{ds(on)}$). In order to judge the performance of MOSFETs, the product of the total gate charge and on-resistance is used as a figure of merit (FOM). Transistors with the same FOM follow the same curve in Figure 5.

Application Information (Cont.)

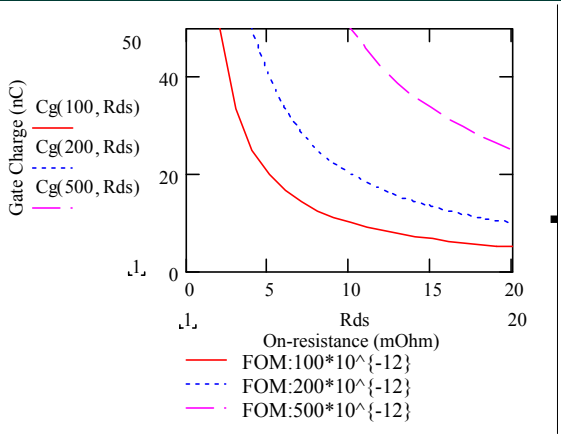


Figure 5. Figure of Merit curves.

The closer the curve is to the origin, the lower is the FOM. This means lower switching loss or lower conduction loss or both. It may be difficult to find MOSFETs with both low C_g and low $R_{ds(on}$. Usually a trade-off between $R_{ds(on}$ and C_g has to be made.

MOSFET selection also depends on applications. In many applications, either switching loss or conduction loss dominates for a particular MOSFET. For buck and buck-boost converters with high input to output voltage ratios, the MOSFET is hard switched but conducts with very low duty cycle. For such applications, MOSFETs with low C_g should be used.

MOSFET power dissipation consists of:
a) conduction loss due to the channel resistance $R_{ds(on)}$,
b) switching loss due to the switch rise time t_r and fall time t_f, and
c) the gate loss due to the gate resistance R_G.

The *RMS* value of the MOSFET switch current is calculated as:

$$I_{Qrms} = I_{dc}\sqrt{D(1+\frac{\delta^2}{12})}$$

The conduction losses are then

$$P_{tc} = I_{Qrms}{}^2 R_{ds(on)}$$

Idc is average inductor current. In buck converter, it is also load current. In buck-boost, it is load current divided by 1-D.

$R_{ds(on)}$ varies with temperature and gate-source voltage. Curves showing $R_{ds(on)}$ variations can be found in manufacturers' data sheet. From the FDS6675 datasheet, $R_{ds(on)}$ is less than 14mΩ when V_{gs} is greater than 10V. However $R_{ds(on)}$ increases by 30% as the junction temperature increases from 25°C to 110°C.

The switching losses can be estimated using the simple formula:

$$P_{ts} = \frac{1}{2}(t_r + t_f)(1+\frac{\delta}{2})I_{dc}V_{in}f_s$$

where t_r is the rise time and t_f is the fall time of the switching process. Different manufacturers have different definitions and test conditions for t_r and t_f. To clarify these, we sketch the typical MOSFET switching characteristics under clamped inductive mode in Figure 6.

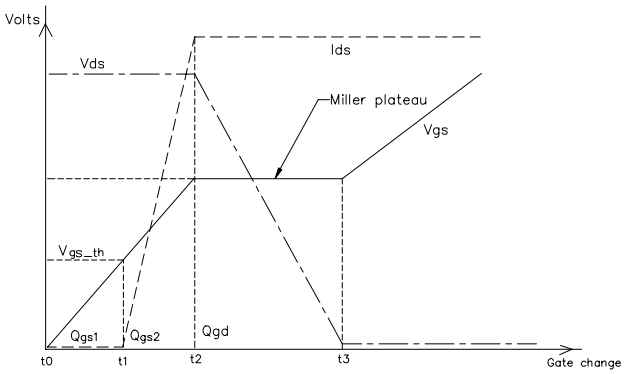


Figure 6. MOSFET switching characteristics

In Figure 6,
Q_{gs1} is the gate charge needed to bring the gate-to-source voltage V_{gs} to the threshold voltage V_{gs_th},
Q_{gs2} is the additional gate charge required for the switch current to reach its full-scale value I_{ds} and
Q_{gd} is the charge needed to charge gate-to-drain (Miller) capacitance when V_{ds} is falling.
Switching losses occur during the time interval [t_1, t_3]. Defining $t_r = t_3 - t_1$ and t_r can be approximated as:

$$t_r = \frac{(Q_{gs2} + Q_{gd})R_{gt}}{V_{cc} - V_{gsp}}$$

where R_{gt} is the total resistance from the driver supply rail to the gate of the MOSFET. It includes the gate driver internal impedance R_{gi}, external resistance R_{ge} and the gate resistance R_g within the MOSFET i.e.

$$R_{gt} = R_{gi} + R_{ge} + R_g$$

V_{gsp} is the Miller plateau voltage shown in Figure 11. Similarly an approximate expression for t_f is:

Application Information (Cont.)

$$t_f = \frac{(Q_{gs2} + Q_{gd})R_{gt}}{V_{gsp}}$$

Only a portion of the total losses ($P_g = Q_g V_{cc} f_s$) is dissipated in the MOSFET package. Here Qg is the total gate charge specified in the datasheet. The power dissipated within the MOSFET package is:

$$P_{tg} = \frac{R_g}{R_{gt}} Q_g V_{cc} f_s$$

The total power loss of the top switch is then:

$$P_t = P_{tc} + P_{ts} + P_{tg}$$

If the input supply of the power converter varies over a wide range, then it will be necessary to weigh the relative importance of conduction and switching losses. This is because conduction losses are inversely proportional to the input voltage. Switching loss however increases with the input voltage. The total power loss of MOSFET should be calculated and compared for high-line and low-line cases. The worst case is then used for thermal design.

Freewheeling Diode Selection

The Schottky diode is recommended as freewheeling diode in the both Buck and Buck-Boost applications. The diode conducts during the off-time. The diode voltage and current ratings are selected based on the peak reverse voltage, the peak current and average power dissipation. The following could be used to determine the diode reversed voltage:

$$V_{D(REV)} = V_{IN}, I_{D(PEAK)} = I_O + \frac{\Delta I_L}{2}, I_{D(AVG)} = I_O \frac{V_{IN} - V_O}{V_{IN} + V_D} \text{ for Buck}$$

$$V_{D(REV)} = V_{IN} + |V_O|, I_{D(PEAK)} = I_O\left(\frac{V_{IN} + |V_O| + V_D}{V_{IN}}\right) + \frac{\Delta I_L}{2}, I_{D(AVG)} = I_O$$

for Buck – Boost

The most stressful condition for the diode occurs when the output is shorted. Under this condition, due to the V_{OUT} = 0, the diode conducts at close to 100% duty cycle. Therefore, attention should be paid to the thermal condition when laying out a board.

Once the power losses (P_{loss}) for the MOSFET and freewheeling diode are known, thermal and package design at component and system level should be done to verify that the maximum die junction temperature ($T_{j,max}$, usually 125°C) is not exceeded under the worst-case condition. The equivalent thermal impedance from junction to ambient (θ_{ja}) should satisfy:

$$\theta_{ja} \le \frac{T_{j,max} - T_{a,max}}{P_{loss}}$$

θ_{ja} depends on the die to substrate bonding, packaging material, the thermal contact surface, thermal compound property, the available effective heat sink area and the air flow condition (free or forced convection). Actual temperature measurement of the prototype should be carried out to verify the thermal design.

Overload Protection and Hiccup

During start-up, the capacitor from the SS/EN pin to ground functions as a soft-start capacitor. After the converter starts and enters regulation, the same capacitor operates as an overload shutoff timing capacitor. As the load current increases, the cycle-by-cycle current-limit comparator will first limit the inductor current. If the over-current persists for more than 32 consecutive switching cycles, the controller will shut off the MOSFETs. Meanwhile an internal 12mA current source discharges the soft-start capacitor C_{SS} connected to the SS/EN pin.

When the capacitor is discharged to 0.5V, a 10µA current source recharges the SS/EN capacitor to 0.9V and driver stage is enabled. Then a 20uA current source continues to charge the soft-start capacitor. As the soft-start capacitor reaches 1.4V, VREF will start to follow the soft-start capacitor voltage until VREF=0.5V. If overload persists, the controller will shut down the converter when the soft-start capacitor voltage exceeds 1.4V. The converter will repeatedly start and shut off until it is no longer overloaded. This hiccup mode of overload protection is a form of foldback current limiting. The following calculations estimate the average inductor current when the converter output is shorted to the ground.

a) The time taken to charge the capacitor from 0.5V to 0.9V

$$t_{ssr1} = C_{SS} \frac{(0.9 - 0.5)V}{10uA}$$

If C_{SS} = 0.1µF, t_{ssr1} is calculated as 4ms.

b) The time to charge the capacitor from 0.9V to 1.4V (driver is enabled but output duty cycle is 0)

Application Information (Cont.)

$$t_{ssr2} = C_{SS}\frac{(1.4-0.9)V}{20\mu A}$$

When C_{SS} = 0.1µF, t_{ssr2} is calculated as 2.5ms. Note that during this period, the converter does not start switching until SS/EN reaches 1.4V.

c) The effective start-up time is:

$$t_{sse} = \frac{32}{200KHz}$$

Assuming inductor current hitting current limit for 32 cycles after SS/EN reaches 1.4V and fs=200KHz. The average inductor current is then:

$$I_{Leff} = I_{LIM}\frac{t_{sse}}{t_{ssr1}+t_{ssr2}}$$

$I_{Leff} \approx 0.025\ I_{LIM}$ and is independent of the soft start capacitor value. The converter will not overheat in hiccup.

Setting the Output Voltage

The non-inverting input of the error amplifier is brought out as a device pin (Pin 9) to which the user can connect Pin 4 or an external voltage reference. A simple voltage divider (R_{o1} at top and R_{o2} at bottom) sets the converter output voltage. In buck converter, the voltage feedback gain (h=0.5/V_o) is related to the divider resistors value as:

$$R_{o2} = \frac{h}{1-h}R_{o1}$$

Once either R_{o1} or R_{o2} is chosen, the other can be calculated for the desired output voltage V_o. Since the number of standard resistance values is limited, the calculated resistance may not be available as a standard value resistor. As a result, there will be a set error in the converter output voltage. This non-random error is caused by the feedback voltage divider ratio. It cannot be corrected by the feedback loop.

The following table lists a few standard resistor combinations for realizing some commonly used output voltages.

Vo (V)	**0.6**	0.9	**1.2**	**1.5**	1.8	2.5	3.3
(1-h)/h	**0.2**	0.8	**1.4**	**2**	2.6	4	5.6
Ro1 (Ohm)	**200**	806	**1.4K**	**2K**	2.61K	4.02K	5.62K
Ro2 (Ohm)	**1K**	1K	**1K**	**1K**	1K	1K	1K

Only the voltages in boldface can be precisely set with standard 1% resistors.

From this table, one may also observe that when the value

$$\frac{1-h}{h} = \frac{V_o - 0.5}{0.5}$$

and its multiples fall into the standard resistor value chart (1%, 5% or so), it is possible to use standard value resistors to exactly set up the required output voltage value.

In buck-boost converter, output voltage is set by

$$R_{o2} = \frac{0.5}{V_O}R_{o1}$$

The input bias current of the error amplifier also causes an error in setting the output voltage. The inverting input bias currents of error amplifiers is -100nA. Since the non-inverting input is biased to 0.5V in buck converter, the percentage error in the second output voltage will be $-100\% \cdot (0.1\mu A) \cdot R_{o1}R_{o2}/[0.5 \cdot (R_{o1}+R_{o2})]$. To keep this error below 0.2%, $R_{o1}//R_{o2} < 10k\Omega$.

Loop Compensation

SC4508A is a current-mode controller. Current-mode control is a dual-loop control system in which the inductor peak current is loosely controlled by the inner current-loop. The higher gain outer loop regulates the output voltage. Since the current loop makes the inductor appear as a current source, the complex high-Q poles of the output LC networks is split into a dominant pole determined by the output capacitor and the load resistance and a high frequency pole. This pole-splitting property of current-mode control greatly simplifies loop compensation.

Application Information (Cont.)

The inner current-loop is unstable (sub-harmonic oscillation) unless the inductor current up-slope is steeper than the inductor current down-slope. For stable operation above 50% duty-cycle, a compensation ramp is added to the sensed-current. In the SC4508A the compensation ramp is made switching frequency dependent. The slope of the compensation ramp is:

$$S_e = 500 * f_s mV$$

The slope of the internal compensation ramp is above the minimal slope requirement for current loop stability and is sufficient for all the applications. With the inner current loop stable, the output voltage is then regulated with the outer voltage feedback loop. A simplified equivalent circuit model of the buck converter with current mode control is shown in Figure 7.

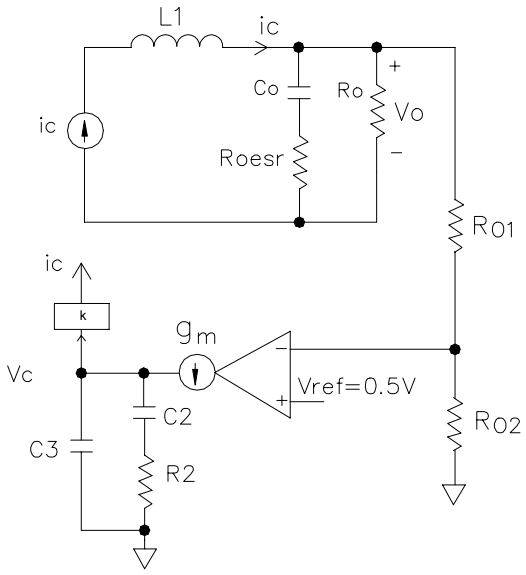


Figure 7. A simple model of buck converter with current mode control.

The transconductance error amplifier (in the SC4508A) has a gain (g_m) of 100µA/V. The target of the compensation design is to select the compensation network consisting of C_2, C_3 and R_2, along with the feedback resistors R_{o1}, R_{o2} and the current sensing gain, such that the converter output voltage is regulated with satisfactory dynamic performance.

With the output voltage V_o known, the feedback gain h and the feedback resistor values are determined using the equations given in the **"Output Voltage Setting"** section with:

$$h = \frac{0.5}{V_o}$$

For the rated output current I_o, the current sensing gain k is fixed as:

$$k = \frac{1}{8 \cdot R_S}$$

From Figure 7, the transfer function from the voltage error amplifier output (v_c) to the converter output (v_o)is:

$$\frac{V_o(s)}{V_c(s)} := G_{vc}(s) = kR_o \frac{1+\frac{s}{s_{z1}}}{1+\frac{s}{s_{p1}}}$$

where, the single dominant pole is:

$$s_{p1} = \frac{1}{(R_o + R_{oesr})C_o}$$

and the zero due to the output capacitor ESR is:

$$s_{z1} = \frac{1}{R_{oesr}C_o}$$

The dominant pole moves as output load varies.

The controller transfer function (from the converter output (v_o) to the voltage error amplifier output (v_c) is:

$$G_c(s) = \frac{g_m}{s(C_2 + C_3)} \frac{1+\frac{s}{s_{z2}}}{1+\frac{s}{s_{p2}}}$$

where

$$s_{z2} = \frac{1}{R_2 C_2}$$

and

$$s_{p2} = \frac{1}{R_2 \frac{C_2 C_3}{C_2 + C_3}}$$

The loop transfer function is then:

$$T(s) = G_{vc}(s) G_C(s) h$$

To simplify design, we assume that $C_3 << C_2$, $R_{oesr} << R_o$, selects $S_{p1} = S_{z2}$ and specifies the loop crossover frequency (f_c). It is noted that the crossover frequency determines the converter dynamic bandwidth. With these

Application Information (Cont.)

assumptions, the controller parameters are determined as follows:

$$C_2 = \frac{g_m k R_o}{2\pi f_c} h$$

$$R_2 = \frac{R_o C_o}{C_2}$$

and

$$C_3 = \frac{R_{oesr} C_o}{R_2}$$

For example, if V_o=3.3V, I_o=2A, f_s=300kHz, C_o=100uF, R_{oesr}=10mΩ, R_s=35mΩ, one can calculate that::

$$R_o = \frac{V_o}{I_o} = 1.65\Omega$$

$$h = \frac{0.5}{V_o} = 0.152$$

and

$$k = \frac{1}{8 \cdot R_S} = 3.57$$

If the converter crossover frequency is set around 1/10 of the switching frequency, f_c = 30kHz, the controller parameters then can be calculated as:

$$C_2 = \frac{g_m k R_o}{2\pi f_c} h \approx 23.6nF$$

where, gm is the error amplifier transconductance gain (100 $\mu\Omega^{-1}$).

If we use C_2 = 22 nF,

$$R_2 = \frac{R_o C_o}{C_2} = 7.5k\Omega$$

use R_2 = 7.5kΩ.
It is further calculated that:

$$C_3 = \frac{R_{oesr} C_o}{R_2} \approx 134pF$$

use C_3 = 120pF. The Bode plot of the loop transfer function (magnitude and phase) is shown in Figure 8.

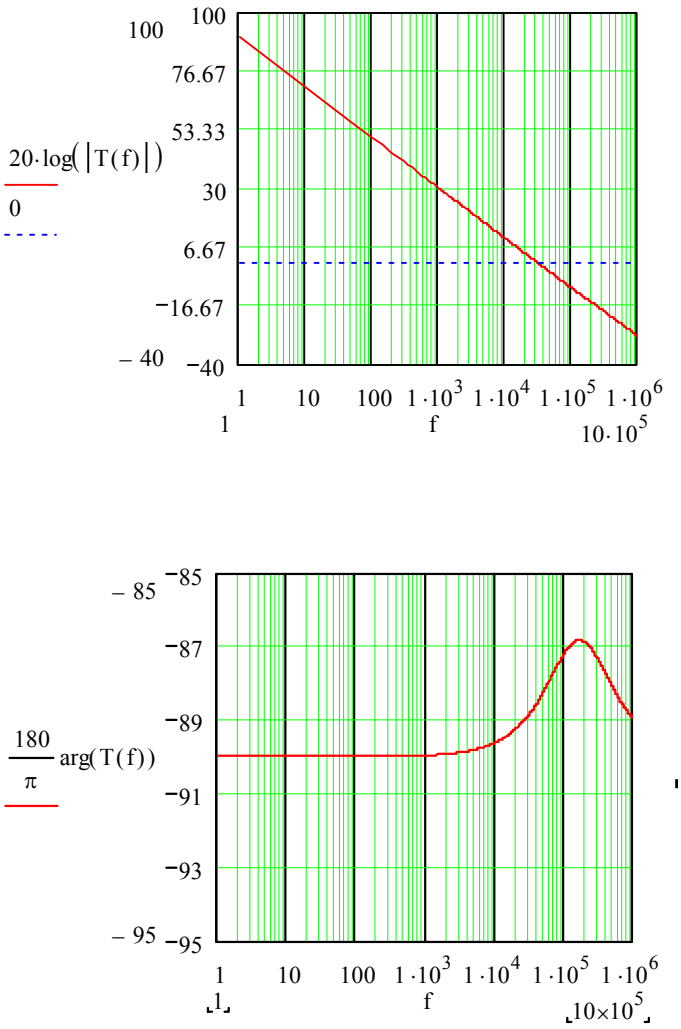


Figure 8. The loop transfer function Bode plot of the buck example.

It is clear that the resulted crossover frequency is about 30*kHz* with phase margin 91°.

For buck-boost converter, a simplified equivalent circuit model of the buck converter with current mode control is shown in Figure 9 and the transfer function from the voltage error amplifier output (v_c) to the converter output (v_o) is:

$$\frac{V_o(s)}{V_c(s)} := G_{vc}(s) = k\frac{1-D}{1+D}R_o\frac{(1-\frac{s}{s_{zRHP}})(1+\frac{s}{s_{z1}})}{1+\frac{s}{s_{p1}}}$$

Application Information (Cont.)

where, the single dominant pole is:

$$s_{p1} = \frac{1+D}{R_o C_o}$$

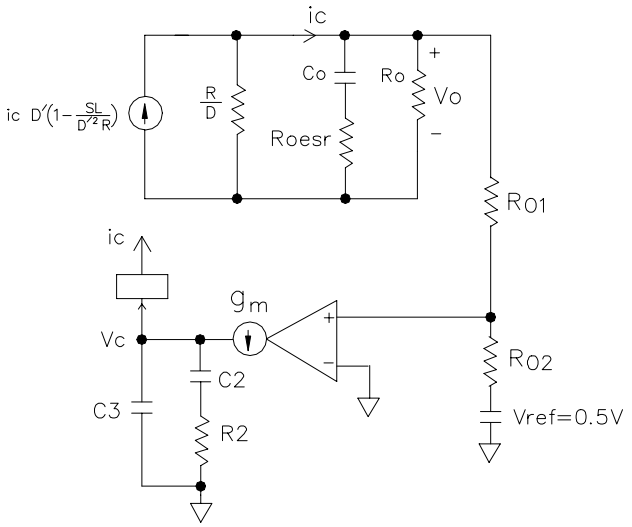


Figure 9. A simple model of buck-boost converter with current mode control.

and the zero due to the output capacitor ESR is:

$$s_{z1} = \frac{1}{R_{oesr} C_o}$$

and the RHP zero associated to the topoly is:

$$s_{zRHP} = \frac{(1-D)^2 \cdot R_o}{D \cdot L}$$

The dominant pole moves as input voltage and output load varies.

The controller transfer function (from the converter output (v_o) to the voltage error amplifier output (v_c) is:

$$G_c(s) = \frac{g_m}{s(C_2 + C_3)} \frac{1 + \frac{s}{s_{z2}}}{1 + \frac{s}{s_{p2}}}$$

where

$$s_{z2} = \frac{1}{R_2 C_2}$$

and

$$s_{p2} = \frac{1}{R_2 \frac{C_2 C_3}{C_2 + C_3}}$$

The loop transfer function is then

$$T(s) = G_{vc}(s) G_C(s) h$$

To simplify design, we assume that $C_3 << C_2$, $R_{oesr} << R_o$, With these assumptions, the controller zero is placed at the converter dominant pole, the controller second pole is placed at the converter ESR zero or RHP zero depending on whichever is lower. The DC gain is finally adjusted for desired phase margin. The controller parameters are determined as following:

Assuming a DC gain ω_I,

$$C_2 = \frac{g_m}{\omega_I}$$

$$R_2 = \frac{1}{C_2 \cdot s_{p1}}$$

and

$$C_3 = \frac{1}{R_2 \cdot s_{z1}} \text{ or } C_3 = \frac{1}{R_2 \cdot s_{zRHP}}$$

For example, if V_{in}=12V, V_o=-12V, I_o=1A, f_s=300kHz, D=0.51, C_o=100uF, R_{oesr}=35mΩ, R_s=35mΩ, one can calculate that::

$$R_o = \frac{V_o}{I_o} = 12\Omega$$

$$h = \frac{0.5}{V_o + 0.5} = 0.04$$

Set ω_I = 500, the controller parameters then can be calculated as:

$$C_2 = \frac{g_m}{\omega_I} h \approx 400nF$$

where, gm is the error amplifier transconductance gain (100 $\mu\Omega^{-1}$).

If we use C_2 = 390 nF,

Application Information (Cont.)

$$R_2 = \frac{1}{s_{p1}C_2} \approx 2.03k\Omega$$

use R_2 = 2kΩ.
Since S_{zRHP}<s_{z1}, it is further calculated that::

$$C_3 = \frac{1}{R_2 \cdot s_{zRHP}} \approx 2.92nF$$

use C_3 = 3.3nF. The Bode plot of the loop transfer function (magnitude and phase) is shown in Figure 10.

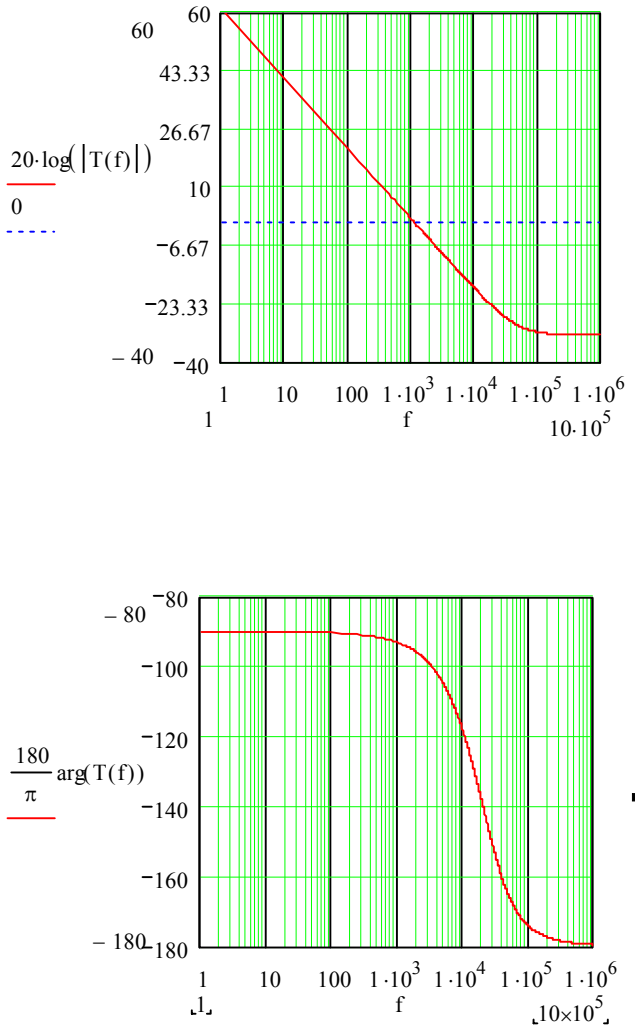


Figure 10. The loop transfer function Bode plot of the buck-boost example.

It is clear that the resulted crossover frequency is about 1*kHz* with phase margin 90°.

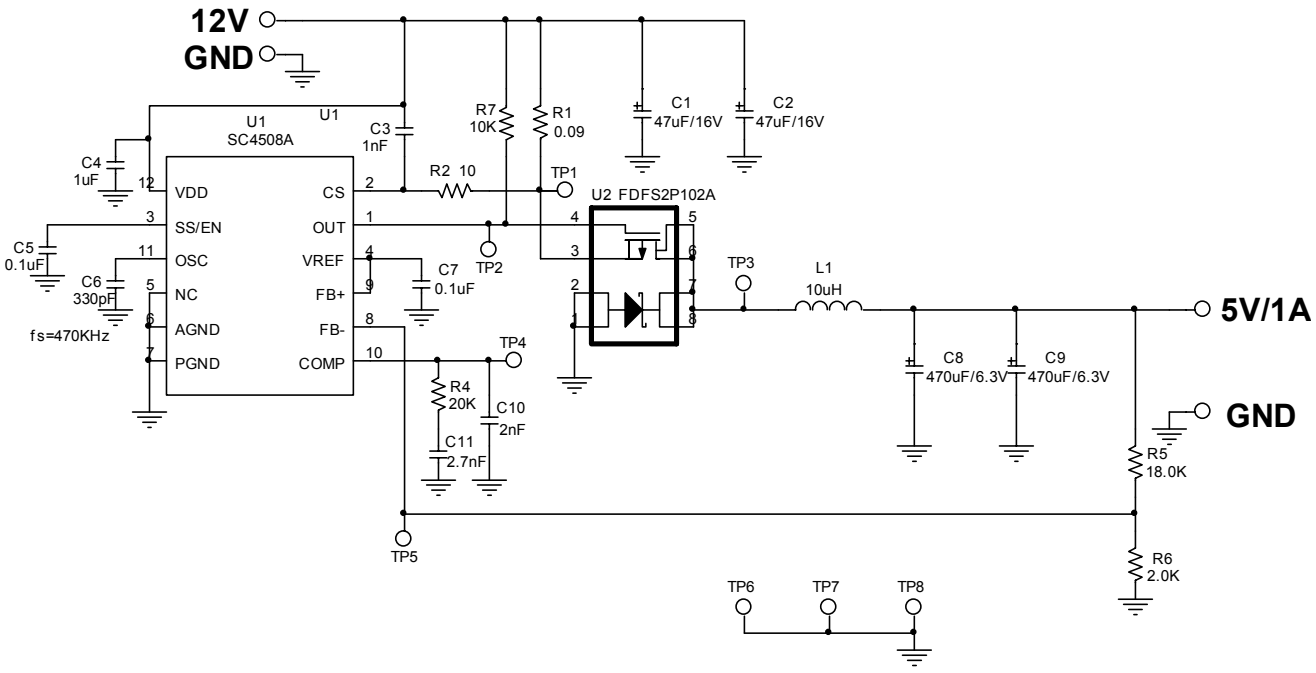
In some initial prototypes, if the circuit noise makes the control loop jitter, it is suggested to use a bigger C_3 value than the calculated one here. Effectively, the converter bandwidth is reduced in order to reject some high frequency noises. In the final working circuit, the loop transfer function should be measured using network analyzer and compared with the design to ensure circuit stability under different line and load conditions. The load transient response behavior is further tested and measured to meet the specification.

Layout Guidelines

In order to achieve optimal electrical, thermal and noise performance for high frequency converters, attention must be paid to the PCB layouts. The goal of layout optimization is to place components properly and identify the high di/dt loops to minimize them. The following guideline should be used to ensure proper functions of the converters.

1. A ground plane is recommended to minimize noises and copper losses, and maximize heat dissipation.
2. Start the PCB layout by placing the power components first. Arrange the power circuit to achieve a clean power flow route. Put all the connections on one side of the PCB with wide copper filled areas if possible.
3. The VDD bypass capacitors should be placed next to the VDD and PGND, AGND pins respectively.
4. Separate the power ground from the signal ground. In SC4508A, the power ground PGND connection should make PFET driving current loop as small as possible. The signal ground AGND should be tied to the negative terminal of the output capacitor.
5. The trace connecting the feedback resistors to the output should be short, direct and far away from the noise sources such as switching node and switching components. Minimize the traces between OUT and the gates of the PFETs to reduce their impedance to drive the MOSFET.
7. Minimize the loop including input capacitors, top/bottom MOSFETs. This loop passes high di/dt current. Make sure the trace width is wide enough to reduce copper losses in this loop.
8. Maximize the trace width of the loop connecting the inductor, PFET and the output capacitors.
9. Connect the ground of the feedback divider and the compensation components directly to the AGND pin of the SC4508A by using a separate ground trace. Then connect this pin to the ground of the output capacitor as close as possible.

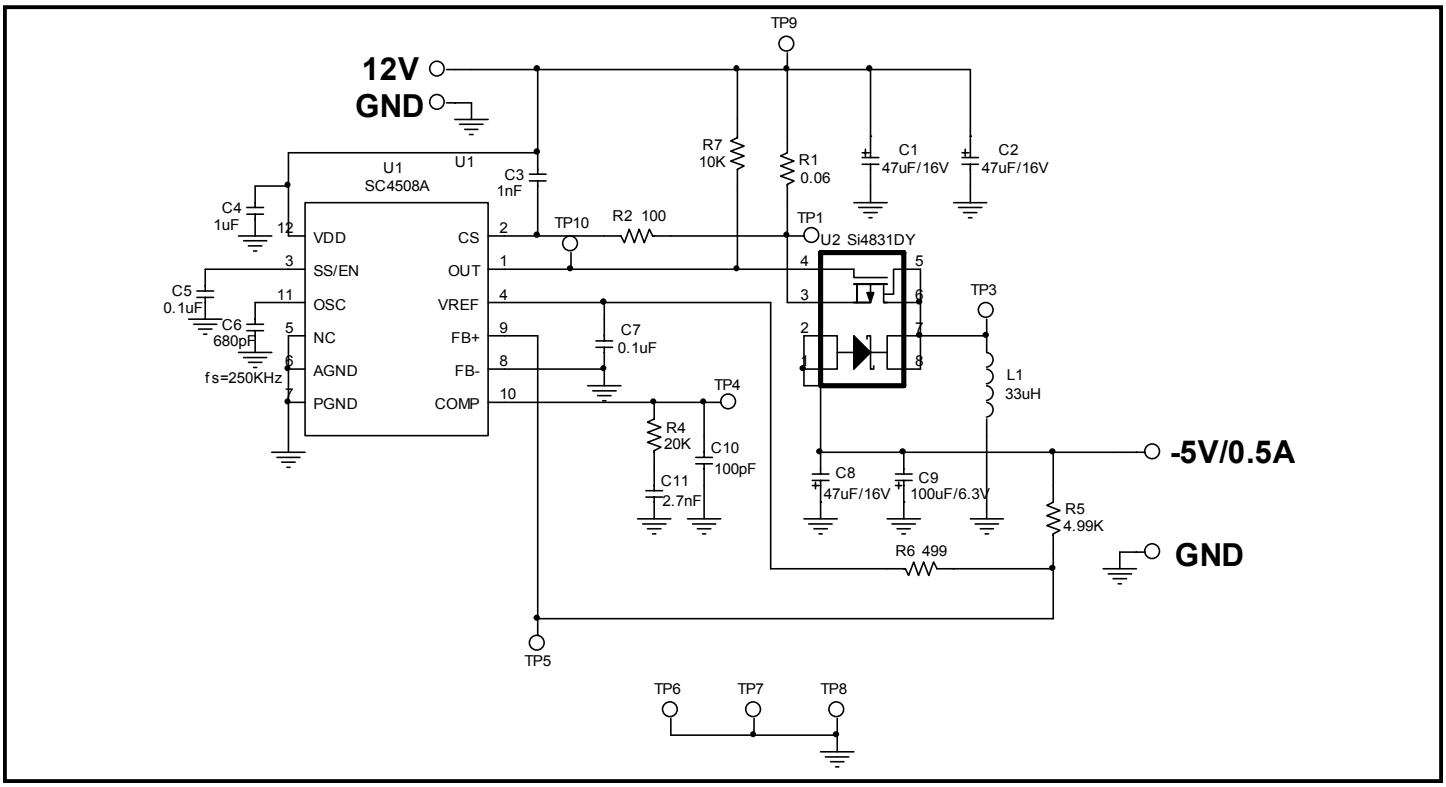
Evaluation Board Schematic, Buck



Bill of Materials

Item	Quantity	Reference	Part	Manufacturer
1	2	C1,C2	47uF/16V	Sanyo P/N: 16TPB47M
2	1	C3	1nF	
3	1	C4	1uF	
4	2	C5,C7	0.1uF	
5	1	C6	330pF	
6	2	C8,C9	470uF/6.3V	Sanyo P/N: 16TPB470M
7	1	C10	2nF	
8	1	C11	2.7nF	
9	1	L1	10uH	
10	1	R1	0.09	
11	1	R2	10	
12	1	R4	20K	
13	1	R5	18.0K	
14	1	R6	2.0K	
15	1	R7	10K	
16	1	U1	SC4508A	Semtech Corp.
17	1	U2	FDFS2P102A	Fairchild P/N: FDFS2P102A

Evaluation Board Schematic, Buck-Boost

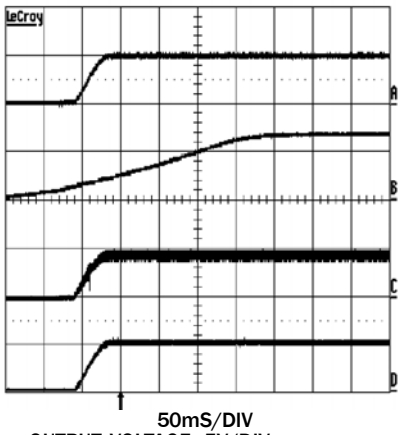


Bill of Materials

Item	Quantity	Reference	Part	Manufacturer
1	3	C1,C2,C8	47uF/16V	Sanyo P/N: 16TPB47M
2	1	C3	1nF	
3	1	C4	1uF	
4	2	C5, C7	0.1uF	
5	1	C6	680pF	
6	1	C9	100uF/6.3V	
7	1	C10	100pF	
8	1	C11	2.7nF	
10	1	L1	33uH	
11	1	R1	0.06	
12	1	R2	100	
13	1	R4	20K	
14	1	R5	4.99K	
15	1	R6	499	
16	1	R7	10K	
19	1	U1	SC4508A	Semtech Corp.
20	1	U2	Si4831DY	Vishay

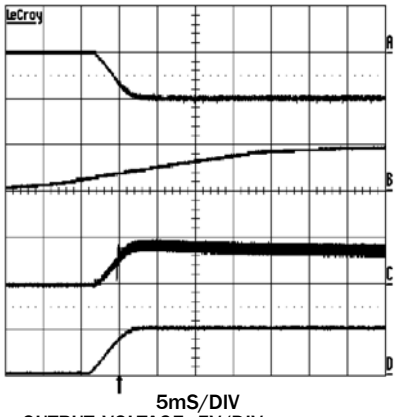
Typical Characteristics

Buck Converter Sartup



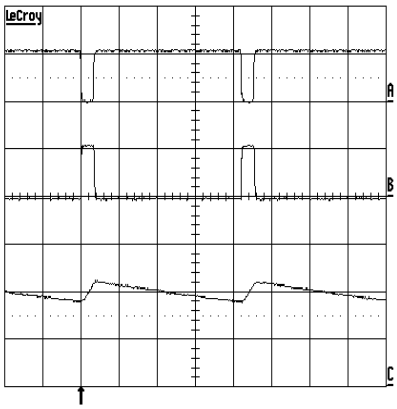
50mS/DIV
a: OUTPUT VOLTAGE, 5V/DIV
b: SS/EN PIN VOLTAGE, 5V/DIV
C: INDUCTOR CURRENT, 2A/DIV
D: VREF PIN VOLTAGE, 0.5V/DIV

Buck-Boost Converter Startup



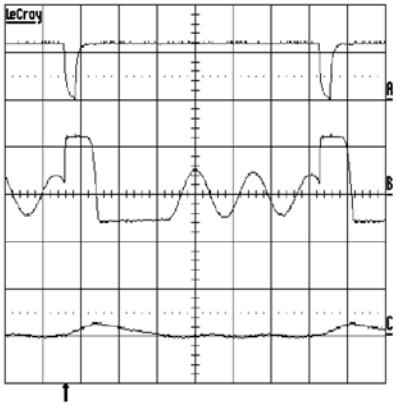
5mS/DIV
a: OUTPUT VOLTAGE, 5V/DIV
b: SS/EN PIN VOLTAGE, 5V/DIV
C: INDUCTOR CURRENT, 2A/DIV
D: VREF PIN VOLTAGE, 0.5V/DIV

Buck CCM Operation



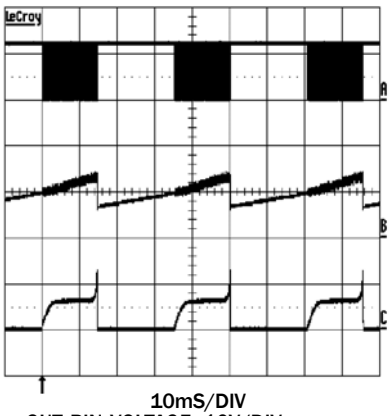
500nS/DIV
a: OUT PIN VOLTAGE, 10V/DIV
b: PHASE NODE VOLTAGE, 10V/DIV
c: INDUCTOR CURRENT, 200mA/DIV

Buck-Boost DCM Operation



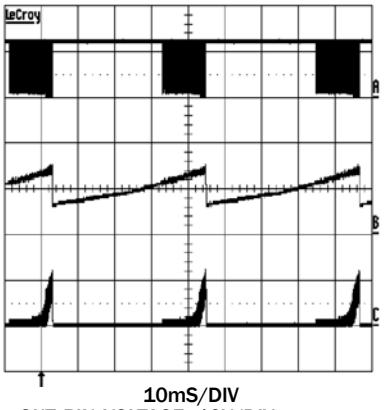
500nS/DIV
a: OUT PIN VOLTAGE, 10V/DIV
b: PHASE NODE VOLTAGE, 10V/DIV
c: INDUCTOR CURRENT, 1A/DIV

Buck Overcurrent Protection



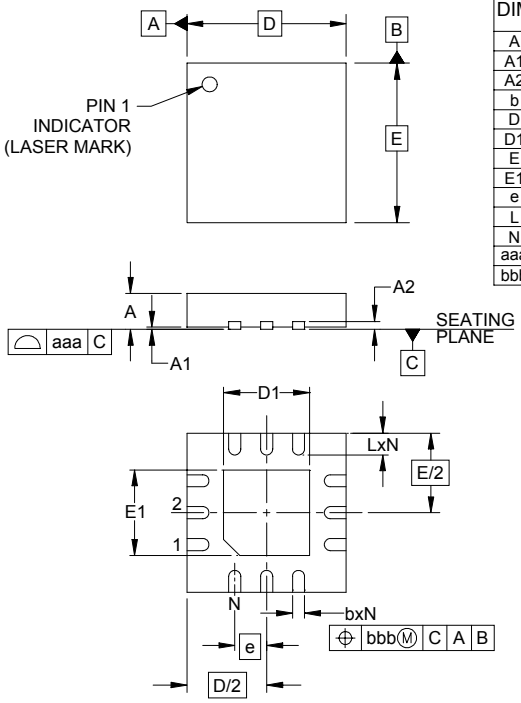
10mS/DIV
a: OUT PIN VOLTAGE, 10V/DIV
b: SS/EN PIN VOLTAGE, 1V/DIV
c: INDUCTOR CURRENT, 2A/DIV

Buck-Boost Overcurrent Protection



10mS/DIV
a: OUT PIN VOLTAGE, 10V/DIV
b: SS/EN PIN VOLTAGE, 1V/DIV
c: INDUCTOR CURRENT, 2A/DIV

Outline Drawing - MLPQ-12, 4 x 4

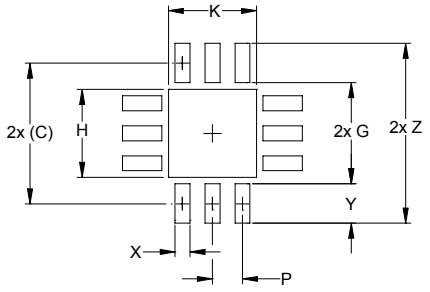


DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	-	.040	0.80	-	1.00
A1	.000	-	.002	0.00	-	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.010	.012	.014	0.25	0.30	0.35
D	.153	.157	.161	3.90	4.00	4.10
D1	.074	.085	.089	1.90	2.15	2.25
E	.153	.157	.161	3.90	4.00	4.10
E1	.074	.085	.089	1.90	2.15	2.25
e	.031 BSC			0.80 BSC		
L	.018	.022	.026	0.45	0.55	0.65
N	12			12		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Land Pattern - MLPQ-12, 4 x 4



DIM	DIMENSIONS	
	INCHES	MILLIMETERS
C	(.148)	(3.75)
G	.106	2.70
H	.091	2.30
K	.091	2.30
P	.031	0.80
X	.016	0.40
Y	.041	1.05
Z	.189	4.80

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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